PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-251564
(43)Date of publication of application : 28.09.1993

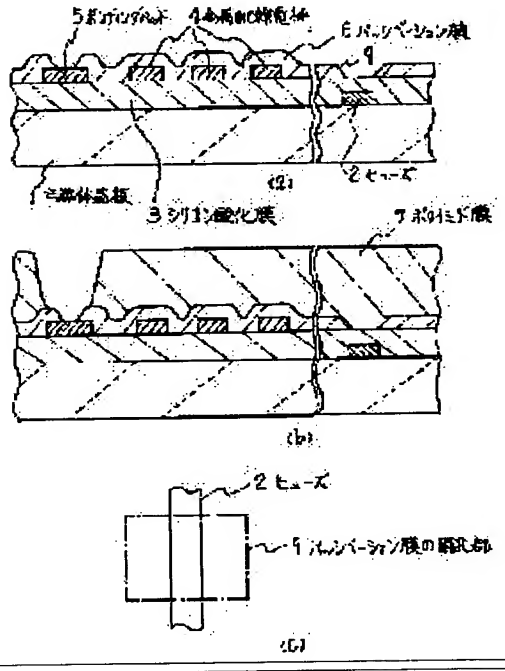
(51)Int.Cl. H01L 21/82
H01L 21/66
H01L 23/02
H01L 23/29
H01L 23/31
H01L 27/10

(21)Application number : 04-038929
(22)Date of filing : 26.02.1992

(71)Applicant : NEC CORP
(72)Inventor : WATANABE KUNIO

(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To prevent the corrosion of a fuse element for redundancy use by applying a thick polyimide film to the fuse element for redundancy use irrespective of whether it is cut or not cut.
CONSTITUTION: A grounding device provided with a bonding pad 5 and a fuse element 2 for redundancy use on a semiconductor substrate 1 is formed and then a passivation film is formed. A silicon oxide film 3 on the bonding pad 5 and the fuse element 2 is disclosed by patterning. After a preliminary electrical characteristic test is performed, the fuse element 2 for redundancy use to be cut is cut by a laser together with the silicon oxide film 3. Polyimide film 7 is applied thereto, and only the bonding pad 5 is disclosed by patterning to expose only the bonding pad 5. Thereby, the fuse element 2 which does not need to be cut is covered with the thick polyimide film 7, so that the moisture resistance thereof may be increased to prevent the corrosion.



LEGAL STATUS

[Date of request for examination] 29.02.1996
[Date of sending the examiner's decision of rejection] 14.07.1998
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]
[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of rejection]
[Date of requesting appeal against examiner's decision of rejection]
[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The manufacture method of a semiconductor device characterized by providing the following. The process which grows a passivation film after forming the ground device which has a pad for bondings, and a fuse element on the main front face of a semiconductor substrate Then, the process which carries out patterning of the aforementioned passivation film, and punctures the aforementioned aforementioned pad for bondings, and fuse element top Then, the process which performs a reserve electrical property examination Then, the process which cuts the required aforementioned fuse element using laser based on the result of the aforementioned reserve electrical property examination, the process which applies the resin film for alpha-rays interception after that, the process which carries out patterning of the aforementioned resin film for alpha-rays interception after that, and punctures only the aforementioned pad for bondings, the process which performs heat treatment after that, and the process which performs an electric examination after that
[Claim 2] The aforementioned fuse element is the manufacture method of the semiconductor device according to claim 1 characterized by being a fuse element for the redundancies of a memory apparatus.
[Claim 3] The aforementioned resin film for alpha-rays interception is the manufacture method of the claim 1 characterized by being a polyimide film, or a semiconductor device according to claim 2.
[Claim 4] It is the manufacture method of the claim 1 characterized by performing the aforementioned heat treatment in nitrogen-gas-atmosphere mind, a claim 2, or a semiconductor device according to claim 3.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the manufacture method of the resin film for alpha-rays interception with respect to the manufacture method of a semiconductor device.
[0002]
[Description of the Prior Art] The manufacture method of the conventional semiconductor device is explained using drawing 2 . The fuse element 2 is formed on the field insulator layer (not shown) formed in the main front face of a semiconductor substrate, and a silicon oxide 3 is formed in the whole. The thickness of the silicon oxide 3 on the fuse element 2 is set to 0.3-0.5 micrometers. And after forming the ground device which formed the pad 5 for bondings, and the metal wiring electrode 4 on the silicon oxide 3 and growing up the passivation film 6 of about 1 micrometer of thickness to be the whole, patterning of this is carried out, puncturing is prepared, the pad 5 for bondings is exposed, and the portion of the silicon oxide 3 on the fuse element 2 is exposed (drawing 2 (a)). Next, the polyimide film 7 used as the resin film for alpha-rays interception is applied to about 8-micrometer thickness, patterning of this is carried out, puncturing is prepared, the pad 5 for bondings is exposed, and the portion of the silicon oxide 3 on the fuse element 2 is exposed (drawing 2 (b)). Next, it heat-treats in nitrogen-gas-atmosphere mind at about 400 degrees C for about 1 hour. In addition, drawing 2 (c) is the plan of the fuse element 2 section, and shows the aperture 9 of the passivation film 6, and the aperture 10 of the polyimide film 7. next, although not shown in drawing, in order to perform a reserve electrical property examination and for this to replace a redundant cell and a poor cell, you should cut -- ** -- the upper shell laser of a silicon oxide 3 cuts the judged fuse element 2 for redundancies, after that, an electrical property examination is performed, the judgment of an excellent article and a defective is performed, and a semiconductor device is completed
[0003]
[Problem(s) to be Solved by the Invention] Thus, by the manufacture method of the conventional semiconductor device, after applying a polyimide film and puncturing the pad for bondings, and fuse element top for redundancies, the fuse element for redundancies is cut. Therefore, since only the silicon oxide whose thickness is 0.3-0.5 micrometers usually existed on this fuse element for redundancies, when a humidity test was performed, the fuse element which is not cut was also corroded, it disconnected and there was a trouble of becoming poor.
[0004]
[Means for Solving the Problem] The process which grows a passivation film after the feature of this invention forms the ground device which has a pad for bondings, and a fuse element on the main front face of a semiconductor substrate, Then, the process which carries out patterning of the aforementioned passivation film, and punctures the aforementioned aforementioned pad for bondings, and fuse element top, Then, the process which performs a reserve electrical property examination and the process which cuts the required aforementioned fuse element after that using laser based on the result of the aforementioned reserve electrical property examination, Then, the process which applies the resin film for alpha-rays interception, for example, a polyimide film Then, it is in the manufacture method of a semiconductor device of having the process which carries out patterning of the aforementioned resin film for alpha-rays interception, and punctures only the aforementioned pad for bondings, the process which performs heat treatment for example, in nitrogen-gas-atmosphere mind after that, and the process which performs an electric examination after that. The aforementioned fuse element can be a fuse element for the redundancies of a memory apparatus here.
[0005]
[Example] Next, this invention is explained with reference to a drawing. Drawing 1 (a) and (b) are drawings of longitudinal section having shown one example of this invention in order of the process, and drawing 1 (c) is the plan of the fuse element section for redundancies of one example of this invention. the field insulator layer (not shown) top first formed in the main front face of a semiconductor substrate like [in drawing 1 (a)] the conventional technology -- the redundancy of a memory apparatus -- the fuse element 2 of business is formed and a silicon oxide 3 is formed in the whole The thickness of the silicon oxide 3 on the fuse element 2 is set to 0.3-0.5 micrometers. And after forming the ground device which formed the pad 5 for bondings, and the metal wiring electrode 4 on the silicon oxide 3 and growing up the passivation film 6 of about 1 micrometer of thickness to be the whole, patterning of this is carried out, puncturing is prepared, the pad 5 for bondings is exposed, and the portion of the silicon oxide 3 on the fuse element 2 is exposed. next, in this invention, although not shown in drawing, in order to perform a reserve electrical property examination and for this to replace a redundant cell and a poor cell, you should cut -- ** -- the upper shell laser of a silicon oxide 3 cuts the judged fuse element 2 for redundancies Next, as shown in drawing 1 (b), the polyimide film 7 used as the resin film for alpha-rays interception is applied to about 8-micrometer thickness, patterning of this is carried out, only on the pad 5 for bondings, puncturing is prepared and only the pad 5 for bondings is exposed (drawing 1 (b)). In addition, drawing 1 (b) shows the fuse element section for redundancies which is not cut. Next, it heat-treats in nitrogen-gas-atmosphere mind at about 400 degrees C for about 1 hour. In addition, drawing 1 (c) is the plan of the fuse element section 2, and shows the aperture 9 of the passivation film 6. Then, an electrical property examination is performed, the judgment of an excellent article and a defective is performed, and a semiconductor device is completed.
[0006]
[Effect of the Invention] as explained above, as compared with the conventional technology, this invention should perform a reserve electrical property examination, before applying a polyimide film, and, thereby, should cut it -- ** -- the upper shell laser of a silicon oxide 3 cuts the judged fuse element 2 for redundancies, it is after that, the polyimide film 7 is applied, patterning of this is carried out, and it is made open [begin] only in the pad for bondings For this reason, the polyimide film exists by about 8-micrometer thick thickness altogether also on the fuse element for redundancies which is not cut on the cut fuse element for redundancies. The effect of it seeming that the fuse element for redundancies which does not have by this the need of cutting is corroded, and it does not become poor was acquired by the humidity test.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

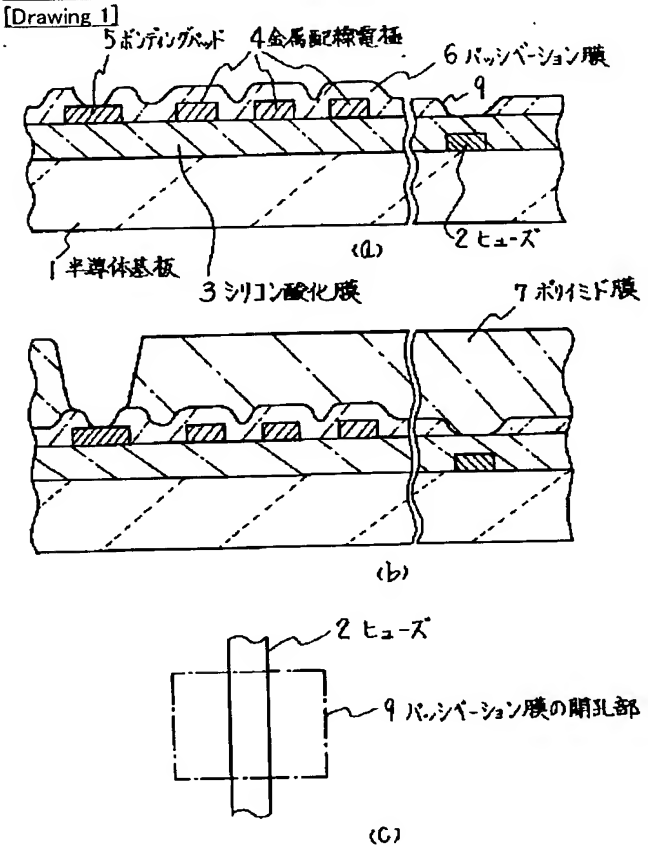
[Brief Description of the Drawings]
[Drawing 1] Drawing showing one example of this invention.
[Drawing 2] Drawing showing the conventional technology.
[Description of Notations]
1 Semiconductor Substrate
2 Fuse Element
3 Silicon Oxide
4 Metal Wiring Electrode
5 Pad for Bondings
6 Passivation Film
7 Polyimide Film
8 Fuse Element
9 Aperture of Passivation Film
10 Aperture of Polyimide Film

[Translation done.]

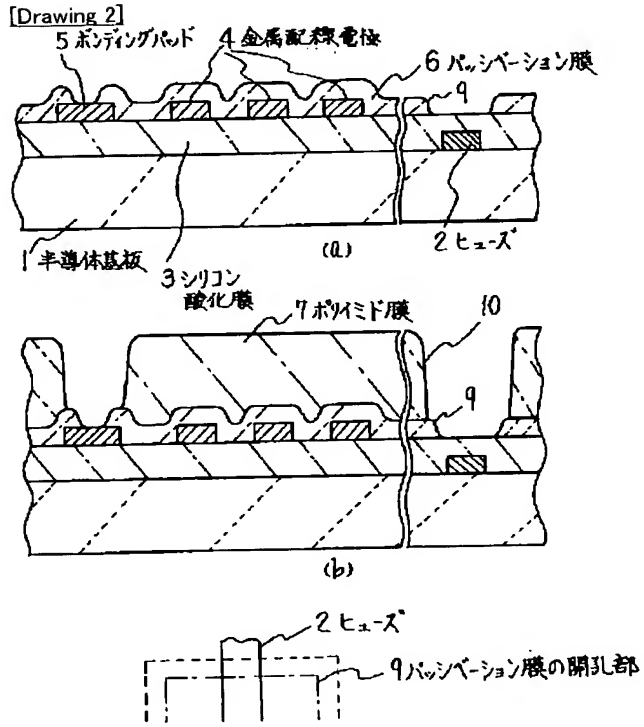
* NOTICES *

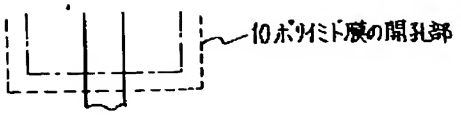
DRAWINGS

[Drawing 1]



[Drawing 2]





(c)

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平5－251564

(43)公開日　平成５年(1993)９月28日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ　21/82				
21/66	Ｚ	8406－4Ｍ		
23/02	Ａ			
		9169－4Ｍ	Ｈ０１Ｌ　21/ 82	Ｒ
		9169－4Ｍ		Ｆ

審査請求　未請求　請求項の数４(全　４　頁)　最終頁に続く

(21)出願番号　特願平4－38929

(22)出願日　平成４年(1992)２月26日

(71)出願人　000004237
日本電気株式会社
東京都港区芝五丁目７番１号

(72)発明者　渡邊　邦生
東京都港区芝五丁目７番１号日本電気株式会社内

(74)代理人　弁理士　京本　直樹　(外２名)

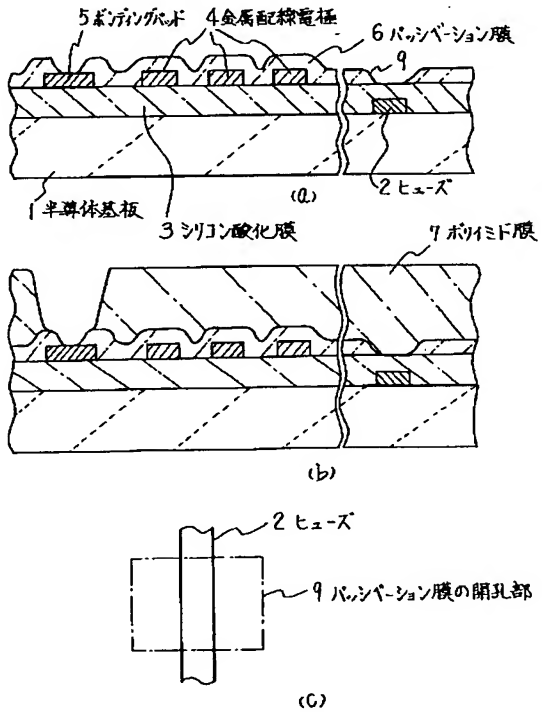
(54)【発明の名称】　半導体装置の製造方法

(57)【要約】

【目的】リダンダンシー用ヒューズ素子の腐食を防止する。

【構成】半導体基板１上にボンディング用パッド５とリダンダンシー用ヒューズ素子２を備えた下地デバイスを形成した後、パッシベーション膜を形成しここにボンディング用パッドとリダンダンシー用ヒューズ素子上のみ開孔し、予備電気的特性試験を行いこれにより必要なリダンダンシー用ヒューズ素子を切断し、しかる後、全体にポリイミド膜を塗布しボンディング用パッド上のに開孔する。

【効果】切断する必要のないリダンダンシー用ヒューズ素子は厚いポリイミド膜によって被覆されているから、耐湿性が向上して腐食が防止される。



1

【特許請求の範囲】

【請求項１】　半導体基板の主表面上にボンディング用パッドとヒューズ素子とを有する下地デバイスを形成した後、パッシベーション膜を成長する工程と、その後、前記パッシベーション膜をパターニングして前記ボンディング用パッドと前記ヒューズ素子上を開孔する工程と、その後、予備電気的特性試験を行う工程と、その後、前記予備電気的特性試験の結果に基いて必要な前記ヒューズ素子をレーザーを用いて切断する工程と、その後、α線遮断用樹脂膜を塗布する工程と、その後、前記α線遮断用樹脂膜をパターニングして前記ボンディング用パッドのみを開孔する工程と、その後、熱処理を行う工程と、その後、電気的試験を行う工程とを有することを特徴とする半導体装置の製造方法。

【請求項２】　前記ヒューズ素子はメモリー装置のリダンダンシー用のヒューズ素子であることを特徴とする請求項１に記載の半導体装置の製造方法。

【請求項３】　前記α線遮断用樹脂膜はポリイミド膜であることを特徴とする請求項１もしくは請求項２に記載の半導体装置の製造方法。

【請求項４】　前記熱処理は窒素雰囲気中で行うことを特徴とする請求項１、請求項２もしくは請求項３に記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は半導体装置の製造方法に係わり、特にα線遮断用樹脂膜の製造方法に関する。

【０００２】

【従来の技術】従来の半導体装置の製造方法を図２を用いて説明する。半導体基板の主表面に形成されたフィールド絶縁膜（図示せず）上にヒューズ素子２を形成し、全体にシリコン酸化膜３を形成する。ヒューズ素子２上のシリコン酸化膜３の膜厚は０．３～０．５μｍとなる。そしてボンディング用パッド５および金属配線電極４をシリコン酸化膜３上に設けた下地デバイスを形成した後、全体に膜厚約１μｍのパッシベーション膜６を成長した後、これをパターニングして開孔を設けボンディング用パッド５を露出させ、ヒューズ素子２上のシリコン酸化膜３の部分を露出させる（図２（ａ））。次に、α線遮断用樹脂膜となるポリイミド膜７を約８μｍの膜厚に塗布し、これをパターニングして開孔を設けボンディング用パッド５を露出させ、ヒューズ素子２上のシリコン酸化膜３の部分を露出させる（図２（ｂ））。次に、約４００℃にて、１時間程度、窒素雰囲気中で熱処理を行う。尚、図２（ｃ）はヒューズ素子２部の平面図であり、パッシベーション膜６の開孔部９とポリイミド膜７の開孔部１０を示す。次に、図には示さないが、予備電気的特性試験を行い、これにより冗長セルと不良セルとを置換する為に、切断すべきと判断されたリダンダンシー用ヒューズ素子２をシリコン酸化膜３の上からレーザーにより切断し、その後、電気的特性試験を行い、良品と不良品の判定を行い半導体装置を完成させる。

2

【０００３】

【発明が解決しようとする課題】このように従来の半導体装置の製造方法では、ポリイミド膜を塗布しボンディング用パッドとリダンダンシー用ヒューズ素子上を開孔した後に、リダンダンシー用ヒューズ素子を切断する。したがってこのリダンダンシー用ヒューズ素子上には通常、膜厚が０．３～０．５μｍのシリコン酸化膜しか存在しないため、耐湿性試験を行った時に、切断しないヒューズ素子も腐食され、断線し、不良になるという問題点があった。

【０００４】

【課題を解決するための手段】本発明の特徴は、半導体基板の主表面上にボンディング用パッドとヒューズ素子とを有する下地デバイスを形成した後、パッシベーション膜を成長する工程と、その後、前記パッシベーション膜をパターニングして前記ボンディング用パッドと前記ヒューズ素子上を開孔する工程と、その後、予備電気的特性試験を行う工程と、その後、前記予備電気的特性試験の結果に基いて必要な前記ヒューズ素子をレーザーを用いて切断する工程と、その後、α線遮断用樹脂膜、例えばポリイミド膜を塗布する工程と、その後、前記α線遮断用樹脂膜をパターニングして前記ボンディング用パッドのみを開孔する工程と、その後、熱処理を、例えば窒素雰囲気中で行う工程と、その後、電気的試験を行う工程とを有する半導体装置の製造方法にある。ここで前記ヒューズ素子はメモリー装置のリダンダンシー用のヒューズ素子であることができる。

【０００５】

【実施例】次に本発明について図面を参照して説明する。図１（ａ），（ｂ）は本発明の一実施例を工程順に示した縦断面図であり、図１（ｃ）は本発明の一実施例のリダンダンシー用ヒューズ素子部の平面図である。まず図１（ａ）では従来技術と同様に、半導体基板の主表面に形成されたフィールド絶縁膜（図示せず）上にメモリー装置のリダンダンシー用のヒューズ素子２を形成し、全体にシリコン酸化膜３を形成する。ヒューズ素子２上のシリコン酸化膜３の膜厚は０．３～０．５μｍとなる。そしてボンディング用パッド５および金属配線電極４をシリコン酸化膜３上に設けた下地デバイスを形成した後、全体に膜厚約１μｍのパッシベーション膜６を成長した後、これをパターニングして開孔を設けボンディング用パッド５を露出させ、ヒューズ素子２上のシリコン酸化膜３の部分を露出させる。次に本発明では、図には示さないが、予備電気的特性試験を行い、これにより冗長セルと不良セルとを置換する為に、切断すべきと判断されたリダンダンシー用ヒューズ素子２をシリコン酸化膜３の上からレーザーにより切断する。次に図１（ｂ）に示す様に、α線遮断用樹脂膜となるポリイミド

3

膜７を約８μｍの膜厚に塗布し、これをパターニングしてボンディング用パッド５上のみに開孔を設けボンディング用パッド５のみを露出させる（図１（ｂ））。尚、図１（ｂ）は切断されないリダンダンシー用ヒューズ素子部を示している。次に、約４００℃にて、１時間程度、窒素雰囲気中で熱処理を行う。尚、図１（ｃ）はヒューズ素子部２の平面図であり、パッシベーション膜６の開孔部９を示す。その後、電気的特性試験を行い、良品と不良品の判定を行い半導体装置を完成させる。

【０００６】

【発明の効果】以上説明したように本発明は、従来技術と比較して、ポリイミド膜を塗布する前に予備電気的特性試験を行い、これにより切断すべきと判断されたリダンダンシー用ヒューズ素子２をシリコン酸化膜３の上からレーザーにより切断し、その後で、ポリイミド膜７を塗布し、これをパターニングしてボンディング用パッドのみを露出させる。このために、切断したリダンダンシー用ヒューズ素子上にも切断しないリダンダンシー用ヒューズ素子上にも全てポリイミド膜が約８μｍの厚い膜

4

厚で存在している。これにより、切断する必要のないリダンダンシー用ヒューズ素子が腐食されて不良となるような事はないという効果が耐湿性試験によって得られた。

【図面の簡単な説明】

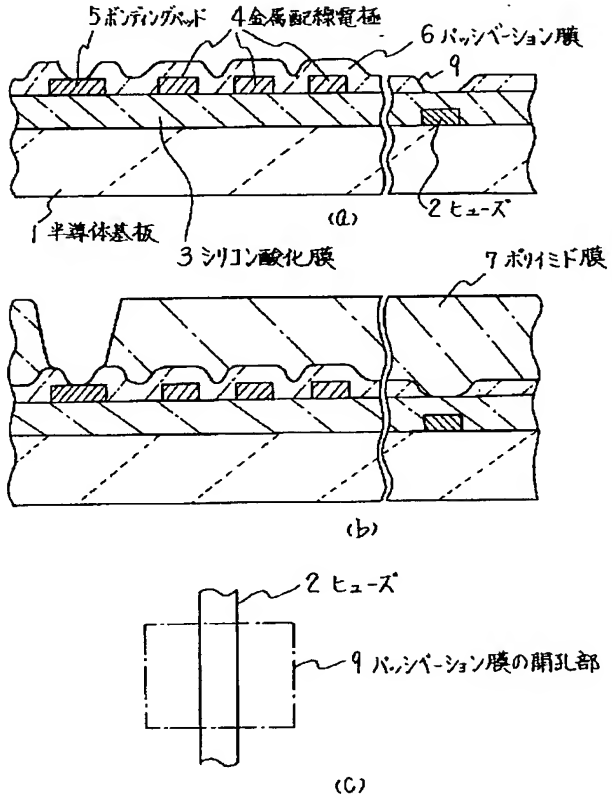
【図１】本発明の一実施例を示す図。

【図２】従来技術を示す図。

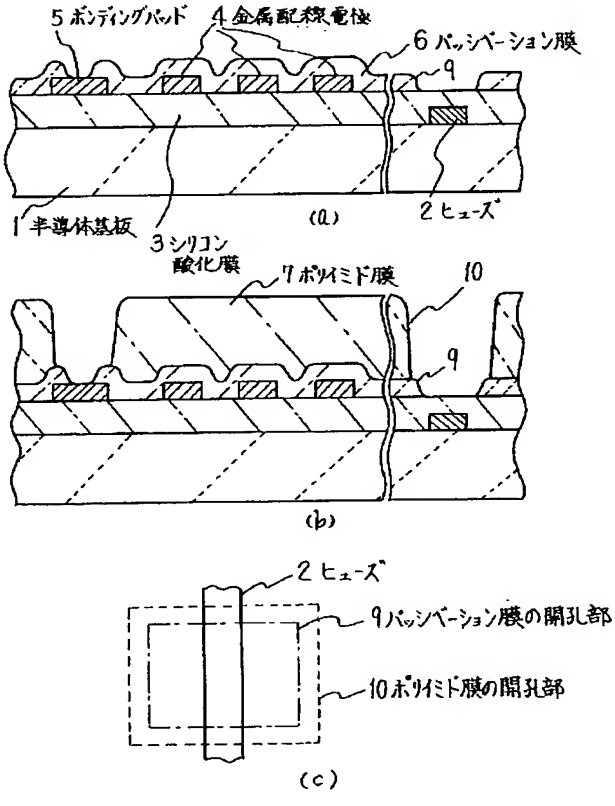
【符号の説明】

１　半導体基板
２　ヒューズ素子
３　シリコン酸化膜
４　金属配線電極
５　ボンディング用パッド
６　パッシベーション膜
７　ポリイミド膜
８　ヒューズ素子
９　パッシベーション膜の開孔部
１０　ポリイミド膜の開孔部

【図１】



【図２】



フロントページの続き

(51)Int.Cl.[5]		識別記号	庁内整理番号	F I		技術表示箇所
Ｈ０１Ｌ	23/29					
	23/31					
	27/10	４９１	8728－4M			
			8617－4M	Ｈ０１Ｌ	23/30	D